

**WHAT IS CLAIMED IS:**

- 1           1.       A method of modeling a combinatorial gate comprising:  
2           providing a data signal input at the combinatorial gate;  
3           providing a clock signal input at the combinatorial gate; and,  
4           propagating the clock signal as an output signal when the output of the  
5                       combinatorial gate corresponds to the clock signal; and,  
6           propagating the data signal as an output when the output of the combinatorial  
7                       gate corresponds to the data signal, the propagating the data signal  
8                       modeling a near domino function.
  
- 1           2.       The method of claim 1 wherein:  
2           the near domino function is propagated based upon performing a reverse  
3                       traversal function on a circuit design containing the combinatorial gate.
  
- 1           3.       The method of claim 1 wherein:  
2           the near domino function includes causing a later arriving edge of the data  
3                       signal to cause the output signal to respond.
  
- 1           4.       The method of claim 1 wherein:  
2           the data signal includes a single edge per clock period; and,  
3           when providing the near domino function, the single edge is propagated  
4                       through the combinatorial gate.
  
- 1           5.       The method of claim 1 wherein:  
2           the clock signal includes two edges per clock period; and,  
3           when propagating the clock signal, the two edges are propagated through the  
4                       combinatorial gate.

1           6.     A method of determining how to model a combinatorial gate where the  
2 combinatorial gate receives a data signal and a clock signal comprising:  
3           performing a reverse traversal function on a circuit containing the  
4           combinatorial gate,  
5           modeling an output of the combinatorial gate as the clock signal when an input  
6           to a next element of the circuit is a clock; and,  
7           modeling the output of the combinatorial gate as a data signal when an input to  
8           a next element of the circuit is a data signal.

9           7.     The method of claim 6 wherein:  
10          the modeling the output of the combinatorial gate as a data signal includes a  
11          near domino function.

1           8.     The method of claim 7 wherein:  
2          the near domino function includes causing a later arriving edge of the data  
3          signal to cause the output signal to respond.

1           9.     The method of claim 7 wherein:  
2          the data signal includes a single edge per clock period; and,  
3          when providing the near domino function, the single edge is propagated  
4          through the combinatorial gate.

1           10.    The method of claim 7 wherein:  
2          the clock signal includes two edges per clock period; and,  
3          when propagating the clock signal, the two edges are propagated through the  
4          combinatorial gate.

- 1           11.    A method of modeling a combinatorial gate within a static timing  
2 analysis comprising:  
3           receiving a data signal at the combinatorial gate;  
4           receiving a clock signal at the combinatorial gate; and,  
5           providing an output corresponding to the clock signal when the output of the  
6           combinatorial gate corresponds to the clock signal; and,  
7           providing an output having a near domino function when the output of the  
8           combinatorial gate corresponds to the data signal.
- 1           12.    The method of claim 11 wherein:  
2           the near domino function is provided based upon performing a reverse  
3           traversal function on a circuit design containing the combinatorial gate.
- 1           13.    The method of claim 11 wherein:  
2           the near domino function includes causing a later arriving edge of the data  
3           signal to cause the output signal to respond.
- 1           14.    The method of claim 11 wherein:  
2           the data signal includes a single edge per clock period; and,  
3           when providing the near domino function, the single edge is propagated  
4           through the combinatorial gate.
- 1           15.    The method of claim 11 wherein:  
2           the clock signal includes two edges per clock period; and,  
3           when providing the clock signal as the output, the two edges are propagated  
4           through the combinatorial gate.

1        16.    A static timing engine comprising:  
 2        a data model, the data model including a combinational block determinator  
 3                module, the combinational block determinator module including  
 4                means for performing a reverse traversal function on a circuit  
 5                        containing the combinatorial gate, and  
 6        a timing engine portion coupled to the data model, the timing engine portion  
 7                including  
 8                means for modeling an output of the combinatorial gate as a clock  
 9                        signal when an input to a next element of the circuit is clock  
 10                        input; and,  
 11                means for modeling the output of the combinatorial gate as a data  
 12                        signal when an input to a next element of the circuit is a data  
 13                        input.

1        17.    The static timing engine of claim 16 wherein:  
 2        the means for modeling the output of the combinatorial gate as a data signal  
 3                includes means for modeling a near domino function.

1        18.    The static timing engine of claim 17 wherein:  
 2        the near domino function includes causing a later arriving edge of the data  
 3                signal to cause the output signal to respond.

1        19.    The static timing engine of claim 17 wherein:  
 2        the data signal includes a single edge per clock period; and,  
 3        when providing the near domino function, the single edge is propagated  
 4                through the combinatorial gate.

1        20.    The static timing engine of claim 17 wherein:  
 2        the clock signal includes two edges per clock period; and,  
 3        when propagating the clock signal, the two edges are propagated through the  
 4                combinatorial gate.